Notice of Allowability	Application No.	Applicant(s)	
	09/820,896	JAIN ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *28 February 2005*.

2. ☒ The allowed claim(s) is/are *1-17*.

3. ☒ The drawings filed on *20 March 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN L. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' response filed on February 28, 2005. Claims 1-17 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone interview with Ms. Molly McCall on March 24, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the Claims:

In claim 1, Lines 7-9, "wherein the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used;"

has been changed to

-- wherein the actual test environment is meant to emulate the actual electronic device in an environment where the actual electronic device will ordinarily be used --.

In claim 1, Lines 14-16, "determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used;"

has been changed to

-- determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used --.

In claim 1, Lines 19-21, "and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used."

has been changed to

-- and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used.--.

In claim 6, Lines 5-6, "wherein the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used;"

has been changed to

-- wherein the actual test environment is meant to emulate the actual electronic device in an environment where the actual electronic device will ordinarily be used --.

In claim 6, Lines 11-13, "determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used;"

has been changed to

-- determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used;--.

In claim 6, Lines 15-17, "and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used."

has been changed to

-- and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used.--.

In claim 11, Lines 6-8, "wherein the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used;"

has been changed to

-- wherein the actual test environment is meant to emulate the actual electronic device in an environment where the actual electronic device will ordinarily be used;--.

In claim 11, Lines 10-12, "and to determine an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used"

has been changed to

-- and to determine an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used --.

In claim 11, Lines 13-15, "and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used are used"

has been changed to

-- and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used are used --.

Reasons for Allowance

4. Claims 1-17 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) an integrated circuit design and evaluation system for evaluating a test pattern produced for the a semiconductor test system, based on logic simulation data produced in the design stage of the IC without using an actual semiconductor test system or the integrated circuit to be tested; the integrated circuit designs are evaluated through a software simulator called device logic simulator; test patterns and expected value patterns for an LSI tester to test the integrated circuits are produced using the dump file produced by the device logic simulator; in device logic simulation, the test patterns to be applied to the device model and the resultant outputs are in an event base; in an actual LSI tester, the test patterns are described in a cycle base; the event base test patterns from the logic simulation are converted to cycle base; an LSI tester simulator is used for evaluating the test patterns; a logic simulator is used for simulating the functions of the device under test which receives the test patterns from the LSI tester simulator (**Matsumura et al.**, U.S. Patent 6,370,675);

(2) a software simulator that simulates the operation of the target chip for cost-effective software development and program verification in non-real time; the simulator simulates the entire target chip and key peripheral features including DMA, timers and serial port etc.; the simulation determines the timings of the device and exactly how the manufactured device will work (**Swoboda et al.,** U.S. Patent 6,704,895); and

(3) a method of analysis of power nets of the integrated circuits; the method uses a transistor network simulator an a power network simulator; the transistor network simulator calculates the current information of the transistor network at specified supply voltages; the power network simulator uses the currents calculated in the transistor network simulation to calculate the node voltages and branch currents in the power net; when the supply voltage drops

below a voltage drop threshold, a timer is started; if the voltage remains below the voltage drop threshold, at the end of a specified amount of time, a voltage drop warning is produced; when the peak current density rises above a peak current density threshold, a timer is started; if the peak current density remains above the peak current density threshold at the end of the specified amount of time, a peak current density warning is produced (**Tuan et al.**, U.S. Patent 5,872,952).

5.1 Applicants' first set of claims consists of claims 1-5.

Independent Claim 1 is directed to a method of evaluating performance of a test environment and an actual electronic device during testing of the actual electronic device. The claim identifies the uniquely distinct features of:

"determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used" and "evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used".

The closest prior art fails to teach or fairly suggest determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used; and evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the

determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used, as claimed by the Applicants. Therefore, claims 1-5 are deemed novel and allowable.

5.2 Applicants' second set of claims consists of claims 6-10.

Independent Claim 6 is directed to an article, comprising a storage medium having instructions stored thereon, the instructions when executed evaluating performance of a test environment and of an actual electronic device during testing of the actual electronic device. The claim identifies the uniquely distinct features of:

"determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used" and "evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used".

The closest prior art fails to teach or fairly suggest determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used and evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the

determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used, as claimed by the Applicants. Therefore, claims 6-10 are deemed novel and allowable.

5.3 Applicants' third set of claims consists of claims 11-17.

Independent Claim 11 is directed to an apparatus for evaluating the performance of a test environment and of an actual electronic device. The claim identifies the uniquely distinct features of:

"to determine an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used wherein the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used are used to evaluate the integrity of the input test signal and a resulting output signal from the virtual device".

The closest prior art fails to teach or fairly suggest to determine an indication of a signal transmission time of the actual electronic device in the environment where the actual electronic device will ordinarily be used wherein the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment where the actual

electronic device will ordinarily be used are used to evaluate the integrity of the input test signal and a resulting output signal from the virtual device, as claimed by the Applicants. Therefore, claims 11-17 are deemed novel and allowable.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
March 24, 2005

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER